IN THE CLAIMS:

Please **amend claims 1-4, 7-10, 12, 13, 15-24, and 26-28** as follows:

1. (*Original*) A transmitter/receiver apparatus comprising:

a plurality of ports of different types;

a bus arbitration circuit that controls timing with which signals are output from the individual ports to a serial bus;

a register in which are stored conditions under which the bus arbitration circuit should operate; and

a delay value optimizing processor that monitors the individual ports and optimizes a transmission delay value of the transmitter/receiver apparatus according to operation status of the individual ports.

2. (*Currently amended*) The transmitter/receiver apparatus according to claim **1**, wherein the delay value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~; and

a reference table that holds, among transmission delay values between the individual ports, maximum values corresponding to different combinations of active ports,

wherein a value read out from the reference table according to an output signal of the status checker is assigned, as the transmission delay value of the transmitter/receiver apparatus, to the register.

3. (*Currently amended*) The transmitter/receiver apparatus according to claim **1**, wherein the delay value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~; and

a reference table that holds whichever are larger between, among transmission delay values between the individual ports, maximum values corresponding to different combinations of active ports and, among transmission delay values required for the individual ports to handle signal input and output singly, maximum values corresponding to different combinations of active ports,

wherein a value read out from the reference table according to an output signal of the status checker is assigned, as the transmission delay value of the transmitter/receiver apparatus, to the register.

4. (*Currently amended*) The transmitter/receiver apparatus according to claim **1**, wherein the delay value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~; and

a reference table that holds, for each of the ports, whichever are larger between, among transmission delay values between the ports excluding that port, maximum values corresponding to different combinations of active ports and a transmission delay value required for that port to handle signal input and output singly,

wherein a value read out from the reference table according to an output signal of the status checker and input port information obtained from the bus arbitration circuit is assigned, as the transmission delay value of the transmitter/receiver apparatus, to the register.

5. (*Original*) A transmitter/receiver apparatus comprising:

a plurality of ports of different types;

a bus arbitration circuit that controls timing with which signals are output from the individual ports to a serial bus;

a register in which are stored conditions under which the bus arbitration circuit should operate; and

a reference table that holds whichever are larger between maximum transmission delay values between the individual ports and maximum transmission delay values required for the individual ports to handle signal input and output singly,

wherein a value read out from the reference table is assigned, as the transmission delay value of the transmitter/receiver apparatus, to the register.

6. (*Original*) A transmitter/receiver apparatus comprising:

a plurality of ports of different types;

a bus arbitration circuit that controls timing with which signals are output from the individual ports to a serial bus;

a first register in which a first operation condition of the bus arbitration circuit is stored;

a second register in which a second operation condition of the bus arbitration circuit is stored;

a delay value optimizing processor that monitors the individual ports and optimizes a transmission delay value of the transmitter/receiver apparatus according to operation status and type of the individual ports.

7. (*Currently amended*) The transmitter/receiver apparatus according to claim **6**, wherein the delay value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~; and

a delay setter that checks for a type of active ports by referring to an output signal of the status checker and to the

second register and that, according to a result of the checking, assigns a transmission delay value stored in the second register to the first register.

8. (*Currently amended*) The transmitter/receiver apparatus according to claim **6**, wherein the delay value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~; and

a delay setter that checks for a type of active ports by referring to an output signal of the status checker and to the second register, that monitors signal lines by way of which the bus arbitration circuit is connected to the first and second registers respectively to check access to the first and second registers from an external node, and that, according to a result of the checking, assigns a transmission delay value stored in the second register to the first register.

9. (*Currently amended*) The transmitter/receiver apparatus according to claim **6**, wherein the delay value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~; and

a delay setter that checks for a type of active ports by referring to an output signal of the status checker and to the second register, that monitors signal lines by way of which the bus arbitration circuit is connected to the first and second registers respectively to check access to the first and second registers from an external node, and that, according to a result of the checking, assigns a transmission delay value stored in the second register to a reply packet returned to the external node.

10. (*Currently amended*) The transmitter/receiver apparatus according to claim **6**, wherein:

a communication line by way of which communication is conducted with the external node complies with the OP i.LINK standard;

the first register is a base register; and

the second register is an OP i.LINK page.

11. (*Original*) A transmitter/receiver apparatus comprising:

a plurality of ports of different types;

a bus arbitration circuit that controls timing with which signals are output from the individual ports to a serial bus;

a register in which are stored conditions under which the bus arbitration circuit should operate; and

a jitter value optimizing processor that monitors the individual ports and optimizes a jitter value of the

transmitter/receiver apparatus according to operation status of the individual ports.

12. (*Currently amended*) The transmitter/receiver apparatus according to claim **11**, wherein the jitter value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~; and

a reference table that holds, among jitter values between the individual ports, maximum values corresponding to different combinations of active ports,

wherein a value read out from the reference table according to an output signal of the status checker is assigned, as the jitter value of the transmitter/receiver apparatus, to the register.

13. (*Currently amended*) The transmitter/receiver apparatus according to claim **11**, wherein the jitter value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~; and

a reference table that holds, for each of the ports, among jitter values between that port and the other ports, maximum values corresponding to different combinations of active ports,

wherein a value read out from the reference table according to an output signal of the status checker and input port information obtained from the bus arbitration circuit is assigned, as the jitter value of the transmitter/receiver apparatus, to the register.

14. (*Original*) A transmitter/receiver apparatus comprising:

a plurality of ports of different types;

a bus arbitration circuit that controls timing with which signals are output from the individual ports to a serial bus;

a first register in which a first operation condition of the bus arbitration circuit is stored;

a second register in which a second operation condition of the bus arbitration circuit is stored;

a jitter value optimizing processor that monitors the individual ports and optimizes a jitter value of the transmitter/receiver apparatus according to operation status and type of the individual ports.

15. (*Currently amended*) The transmitter/receiver apparatus according to claim **14**, wherein the jitter value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~; and

a jitter setter that checks for a type of active ports by referring to an output signal of the status checker and to the second register and that, according to a result of the checking, assigns a jitter value stored in the second register to the first register.

16. (*Currently amended*) The transmitter/receiver apparatus according to claim **14**, wherein the jitter value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~; and

a jitter setter that checks for a type of active ports by referring to an output signal of the status checker and to the second register, that monitors signal lines by way of which the bus arbitration circuit is connected to the first and second registers respectively to check access to the first and second registers from an external node, and that, according to a result of the checking, assigns a jitter value stored in the second register to the first register.

17. (*Currently amended*) The transmitter/receiver apparatus according to claim **14**, wherein the jitter value optimizing processor includes:

a status checker that checks whether the individual ports are active or not; and

a jitter setter that checks type of active ports by referring to an output signal of the status checker and to the second register, that monitors signal lines by way of which the bus arbitration circuit is connected to the first and second registers respectively to check access to the first and second registers from an external node, and that, according to a result of the checking, assigns a jitter value stored in the second register to a reply packet returned to the external node.

18. (*Currently amended*) The transmitter/receiver apparatus according to claim **14**, wherein:

a communication line by way of which communication is conducted with the external node complies with the OP i.LINK standard;

the first register is a base register; and

the second register is an OP i.LINK page.

19. (*Currently amended*) The transmitter/receiver apparatus according to claim **1**, wherein the delay value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~;

a reference table that holds transmission delay values between the individual ports; and

a delay selector that selects, according to an output signal of the status checker, a maximum transmission delay value between active ports from among all the transmission delay values stored in the reference table, and that then assigns the selected value to the register.

20. (*Currently amended*) The transmitter/receiver apparatus according to claim **1**, wherein the delay value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~;

a reference table that holds transmission delay values between the individual ports and transmission delay values required for the individual ports to handle signal input and output singly; and

a delay selector that selects, according to an output signal of the status checker, a maximum transmission delay value involving an active port from among all the transmission delay values stored in the reference table, and that then assigns the selected value to the register.

21. (*Currently amended*) The transmitter/receiver apparatus according to claim **1**, wherein the delay value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~;

a reference table that holds transmission delay values between the individual ports and transmission delay values required for the individual ports to handle signal input and output singly; and

a delay selector that selects, according to an output signal of the status checker and input port information obtained from the bus arbitration circuit, a largest of transmission delay values between active ports other than a signal input port and a transmission delay value required for the signal input port to handle signal input and output singly from among all the transmission delay values stored in the reference table, and that then assigns the selected value to the register.

22. (*Currently amended*) The transmitter/receiver apparatus according to claim **11**, wherein the jitter value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~;

a reference table that holds jitter values between the individual ports; and

a jitter selector that selects, according to an output signal of the status checker, a maximum jitter value between active ports from among all the jitter values stored in the reference table, and that then assigns the selected value to the register.

23. (*Currently amended*) The transmitter/receiver apparatus according to claim **11**, wherein the jitter value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~;

a reference table that holds jitter values between the individual ports; and

a jitter selector that selects, according to an output signal of the status checker and input port information obtained from the bus arbitration circuit, a maximum jitter value between a signal input port and other active ports from among all the jitter values stored in the reference table, and that then assigns the selected value to the register.

24. (*Currently amended*) The transmitter/receiver apparatus according to claim **1**, wherein the delay value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~;

a reference table that holds, for each of the ports, a transmission delay value through that port and through a signal format converter for that port; and

a delay calculator that selects, according to an output signal of the status checker, two largest from among transmission delay values through active ports stored in the reference table, that then adds together the two values and a maximum transmission delay value required for signal processing in a physical layer, and that then assigns a sum thereof to the register.

25. (*Original*) A transmitter/receiver apparatus comprising:

a plurality of ports of different types;

a bus arbitration circuit that controls timing with which signals are output from the individual ports to a serial bus;

a register in which are stored conditions under which the bus arbitration circuit should operate;

a reference table that holds, for each of the ports, a transmission delay value through that port and through a signal format converter for that port; and

a delay calculator that compares a transmission delay value obtained by adding together two largest of the transmission delay values stored in the reference table with a transmission delay value required for a given port to handle signal input and output singly, that then adds to whichever of the two values is larger a maximum

transmission delay value required for signal processing in a physical layer, and that then assigns a sum thereof to the register.

26. (*Currently amended*) The transmitter/receiver apparatus according to claim **1**, wherein the delay value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~;

a reference table that holds, for each of the ports, a transmission delay value through that port and through a signal format converter for that port; and

a delay calculator that compares, according to an output signal of the status checker and input port information obtained from the bus arbitration circuit, a transmission delay value obtained by adding together two largest of transmission delay values through active ports excluding a signal input port stored in the reference table with a transmission delay value required for the signal input port to handle signal input and output singly, that then adds to whichever of the two values is larger a maximum transmission delay value required for signal processing in a physical layer, and that then assigns a sum thereof to the register.

27. (*Currently amended*) The transmitter/receiver apparatus according to claim **11**, wherein the jitter value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~;

a reference table that holds, for each of the ports, a jitter value through that port and through a signal format converter for that port; and

a jitter calculator that selects, according to an output signal of the status checker, two largest from among jitter values through active ports stored in the reference table, that then adds together the two values and a maximum jitter value required for signal processing in a physical layer, and that then assigns a sum thereof to the register.

28. (*Currently amended*) The transmitter/receiver apparatus according to claim **11**, wherein the jitter value optimizing processor includes:

a status checker that checks ~~whether the~~ for active individual ports ~~are active or not~~;

a reference table that holds, for each of the ports, a jitter value through that port and through a signal format converter for that port; and

a jitter calculator that adds together, according to an output signal of the status checker and input port information obtained from the bus arbitration circuit, a jitter value required for a signal input port to handle signal input and output singly, a maximum jitter value through active ports excluding the signal input port stored in the reference table, and a maximum jitter value required for signal processing in a physical layer, and that then assigns a sum thereof to the register.

29. (*Original*) The transmitter/receiver apparatus according to claim **1**, wherein a communication line by way of which communication is conducted with an external node complies with one of IEEE Std. 1394a-2000, IEEE Std. 1394b, or the OP i.LINK standard.

30. (*Original*) The transmitter/receiver apparatus according to claim **5**, wherein a communication line by way of which communication is conducted with an external node complies with one of IEEE Std. 1394a-2000, IEEE Std. 1394b, or the OP i.LINK standard.

31. (*Original*) The transmitter/receiver apparatus according to claim **11**, wherein a communication line by way of which communication is conducted with an external node complies with one of IEEE Std. 1394a-2000, IEEE Std. 1394b, or the OP i.LINK standard.

32. (*Original*) The transmitter/receiver apparatus according to claim **25**, wherein a communication line by way of which communication is conducted with an external node complies with one of IEEE Std. 1394a-2000, IEEE Std. 1394b, or the OP i.LINK standard.